ABSTRACT OF THE DISCLOSURE

[0040] An EEPROM memory cell uses PMOS type floating gate transistor formed in a n-well, where the floating gate is routed over a p- diffused region formed in the n-well to form a control capacitor. The PMOS floating gate transistor uses a p-type diffused region below the p+ active region forming the drain to provide a higher breakdown voltage. Cell programming can be performed through hot-electron injection, with the electric field across the control capacitor to aid injection into the floating gate. FN erasure is achieved by taking the potential of the n-well to the programming voltage while holding the potential of the control capacitor at a low voltage.